Lehrstuhl für Schaltungsentwurf
Fakultät für Elektrotechnik und Informationstechnik
Technische Universität München

Scientific Seminar on Structure, Architecture, and Application of Sensor Circuits

Chair of Circuit Design

Winter Semester 2024

What you will learn in this seminar …

- At least 50% of this seminar is about the soft skills you need to become a successful engineer in science, but also in industry
- You will learn to:
  - Research state-of-the-art for a newly defined problem, and get a deeper understanding of the problem
  - Formulate a plan for solving the problem
  - Present technical work in a scientific paper, such that others can understand the content but also the motivation for the topic, what others have done in the field already, what you did new and better than others, as well as the remaining challenges after your work
  - Orally present the same topic to a group with the same intention

… **good work is often only recognized if it is also well presented (and for this, first of all,** it needs to be understood by others in a short time frame)!

Outline – Kick-Off Meeting

Today …

- Your work and duties during this seminar
- Timing & Deadlines: Submissions and presentations
- Grading of your work
- Presentation of topics by supervisors
- Selection of one topic per student
- Lecture: how to do research

Outline – Course of the seminar

- Then …
  - Lecture 1: How to write an article
  - Lecture 2: How to do a presentation
  - Work on your own: Text / Internet search / discussions
  - In case you need help: please contact your supervisor in advance and try to use your and his/her time efficiently
  - Take advantage of the supervisor's feedback, this is where you can learn most!
  - Show your results: report (4 pages) and oral presentation (12+3 min.)

Your work and duties

- Choose one of the topics
- Do research about the topic
- Write a scientific paper about the topic (4 pages)
- Prepare and give a scientific presentation (12 min + 3 min Q&A, this is the standard for conferences)
- For paper and presentation:
  - focus on basics of the problem and specific implementation
  - a template will be provided on Moodle

Your work and duties

1. Do a literature search and discuss your research results with your supervisor
2. Then study the literature (modified by supervisor)
3. Develop an outline (content) for your paper and presentation
4. Discuss your outline with your supervisor (by appointment)
5. Work out the (modified) outline in your paper
6. Submit your paper
7. Summarize your results in a presentation
8. Submit the presentation

Grading

- ✓ Regular discussions (online/in presence) with the assigned supervisor about the progress of the work and the procedure
- ✓ Oral presentation of the results (12 min.) with subsequent discussion (3 min.) (50%)
- ✓ Scientific paper in IEEE style (4 pages): written elaboration of the results (50%)

Timing & Deadlines

	When?	What?
Kick-off	15.10.2024 (Tuesday) 16:00-18:00	Introduction & How to do a literature research **Participation is mandatory!**
Lecture 1	04.12.2024 (Wednesday) 17:00-18:30	How to write a scientific article
Lecture 2	08.01.2025 (Wednesday) 17:00-18:30	How to prepare and hold a presentation
Paper submission deadline	20.01.2025 (Monday) until 23:59 PM	In Moodle and via email to your supervisor
Presentations *(planned)*	28.01.2025 (Tuesday) & 29.01.2025 (Wednesday) 16:30-18:00	

Topics (Overview)

Topic	Supervisor	Available
Power-on-Reset and Brown-out Detection Circuits	Moritz Gruber	
Wearable Ultrasonic Blood Pressure Monitor	Pengcheng Xu	
Low Power and High Efficiency DC/DC	Pengcheng Xu	
High Voltage BSIM Models Adaptation for Cryogenic Temperatures	Mohammad Abu Zahra	
CFET Architecture for CMOS Scaling Beyond N2	Emanuele Groppo	
Dynamic Offset cancellation techniques: Chopping vs Auto zeroing	Vartika Verma	
Physical Unclonable Functions	Egla Derraj	
Physical Layer RF Fingerprinting for wireless	Egla Derraj	
CD-Converter: Techniques, Efficiency, Flexibility	Tobias Chlan	
Electronic Tongues and Noses	Eva Korek	
Cryogenic Circuit Design for Quantum Computing	Leon Dixius	
Low Distortion Switches for Sample-and-Hold Stages	Leon Dixius	
Neuromorphic Solutions for Control Problems	Ferdinand Pscheidl	

LAST UPDATED 27.09.2024

Supervisor: moritz.gruber@tum.de

Power-on-Reset and Brown-out Detection Circuits

State-of-the-Art Techinques

Background:
Many systems need a defined behavior during start-up and shut-down. Power-on-Reset and Brown-out Detection circuits provide defined voltages/logic-levels during all supply voltages regimes, which can be used for initialization. Since these circuits constantly monitor the supply voltage and can therefore not be turned off, their power consumption is critical.

Tasks:

- Access the need of start-up circuits for initialization and shut-down of digital and analog circuits.
- Compare the State-of-the-Art of start-up circuits:
  - Find different topologies and techniques (e.g. resistor less, capacitive based).
  - Compare topologies and find tradeoffs (e.g. power consumption, area, …).

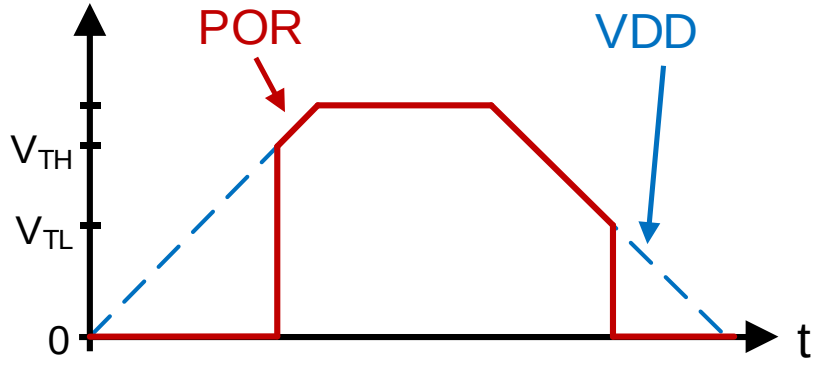


Figure 1. Startup behavior of a Power-on-Reset (POR) circuit. At VDD > V_{TH} the POR triggers. The Brown-out Detection triggers at V_{TL} (< V_{TH}).

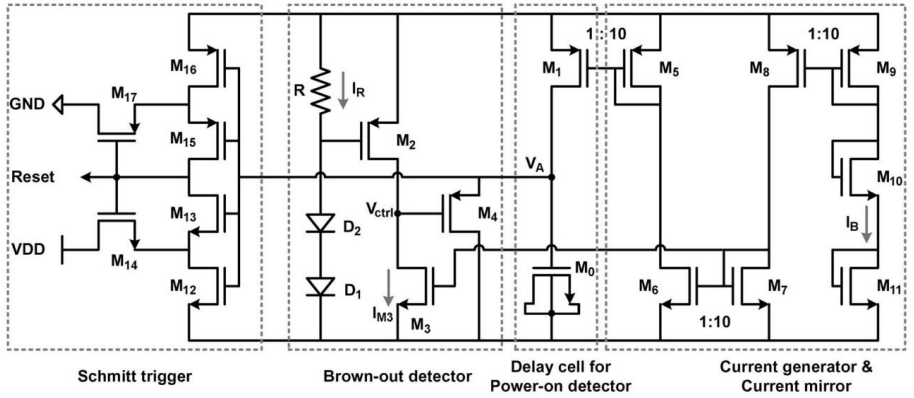


Figure 2. Example circuit of a Power-on-Reset (POR) circuit with Brown-out Detection.

Source Figure 2: Le, Huy-Binh, et al. "A long reset-time power-on reset circuit with brown-out detection capability." IEEE Transactions on Circuits and Systems II.

Supervisor: pengcheng.xu@tum.de

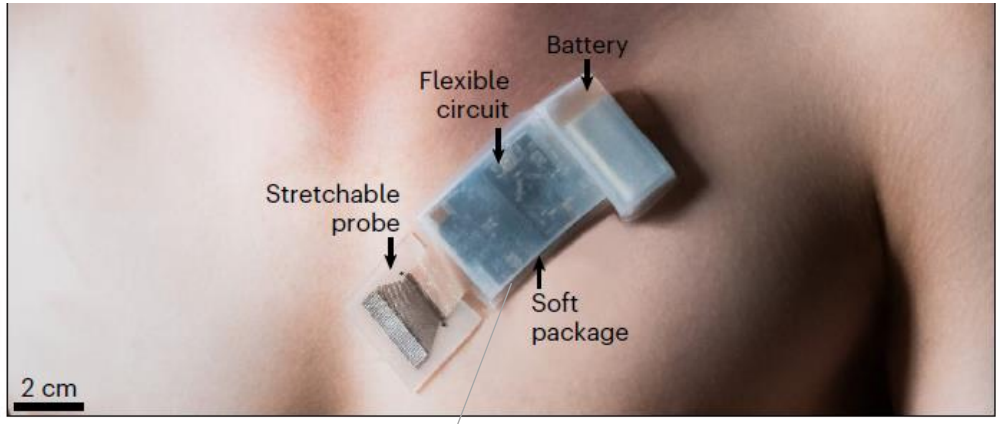
Wearable Ultrasonic Blood Pressure Monitor

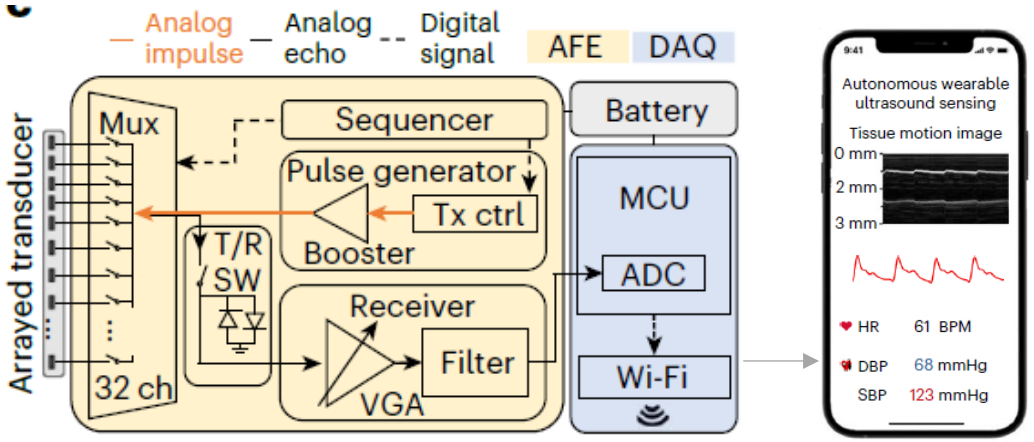
Working Principle Summary and SOA Analysis

Compared with other medical imaging methods, such as X-ray computed tomography and magnetic resonance imaging, ultrasonography is safer, less expensive and more versatile. Common ultrasound probes are bulky and wired to large control systems, which limits their usage to centralized facilities. A fully integrated autonomous ultrasonic system-on-patch (USoP) could be a solution for a wearable blood pressure monitor.

In this topic, you are expected to

- Summary the working principle of ultrasonic blood pressure monitor in algorithm and circuits block levels.
- Categorize existing technologies on low-power integrated ultrasonic blood pressure monitor.
- Analysis the advantage and limitation of the state-of-art works.





Lin, M., Zhang, Z., Gao, X., Bian, Y., Wu, R.S., Park, G., Lou, Z., Zhang, Z., Xu, X., Chen, X. and Kang, A., 2024. A fully integrated wearable ultrasound system to monitor deep tissues in moving subjects. *Nature Biotechnology*, *42*(3), pp.448-457.

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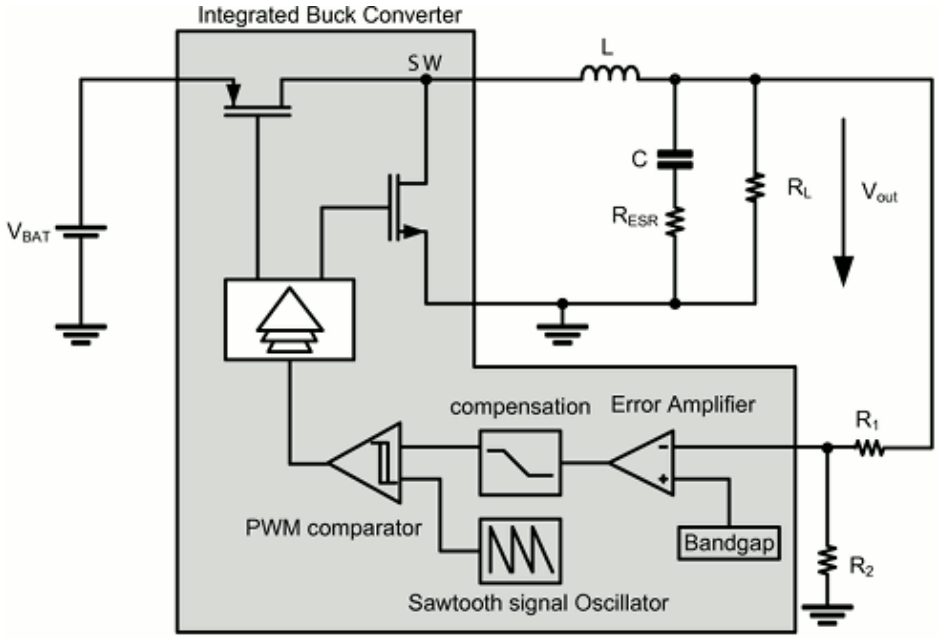
Low Power and High Efficiency DC/DC

Working Principle Summary and SOA Analysis

As these applications of edge AI accelerators, low-power IoT sensors and wearable devices are often deployed in environments with limited power resources, the DC/DC converters must deliver precise voltage regulation with minimal energy loss.

In this topic, you are expected to

- Summary the special requirements of DC/DC used in edge low power devices.
- Summary the working principle of improving DC/DC power efficiency at both heavy and light load.
- Categorize existing technologies on adaptive biasing current based on load condition.
- Analysis the advantage and limitation of the state-of-art works on low-power and high efficiency DC/DC.



Lei Liao. "High efficiency low power DC to DC converters for battery powered portable applications." *RWTH, 2024*

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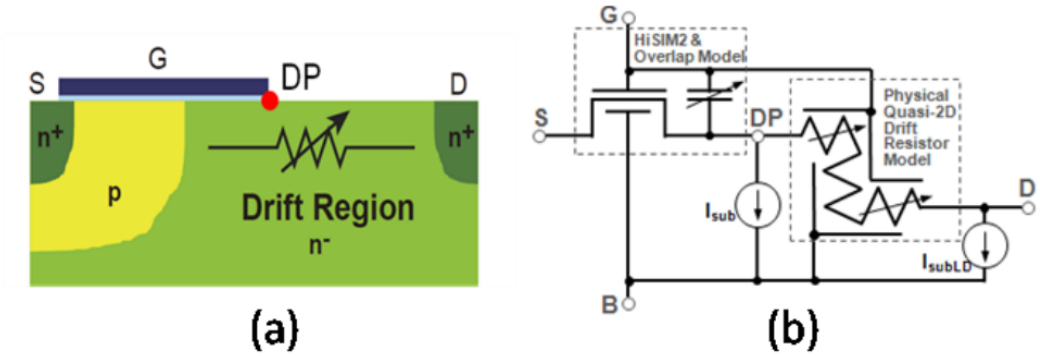
High Voltage BSIM Models Adaptation for Cryogenic Temperatures

Background:

BSIM compact models are used to capture the behaviour of the devices and help simulate circuits. There are several flavours of BSIM models for different types of devices. High voltage devices for example are modelled using BSIM-HV.

As the applications for cryogenic circuit continue to rise, the importance of models that capture the cryogenic behaviour of different devices becomes more apparent. In contrast to CMOS technology, high voltage technology did not have as much interest to model its cryogenic behaviour. However, the importance of high voltage devices at cryogenic temperatures is becoming more apparent. Therefore, understanding the exisiting models and how can they be adjusted for cryogenic operation is a good first step to fully capture high voltage device's cryogenic behaviour,



(a) Simplified LDMOS Structure (b) simplified HiSIM_HV2 equivelant circuit structure

Focus:

- Identify the various flavour of BSIM models used to capture high voltage devices
- Identify the various parameters that would need to be altered for cryogenic operation
- Evaluate the extendibility of existing models to cryogenic temperatures

Mattausch, H.J. & Umeda, T & Kikuchihara, H & Miura-Mattausch, M. (2014). Accurate Physical Compact Models of High-Voltage/Power Semiconductor Devices for Efficient Design of Performance-Optimized Circuits and Systems. 10.7567/SSDM.2014.N-8-1.

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CFET Architecture for CMOS Scaling Beyond N2

Problem:
Exploiting the vertical direction to enable further scaling with stacked n- and p-type channel devices

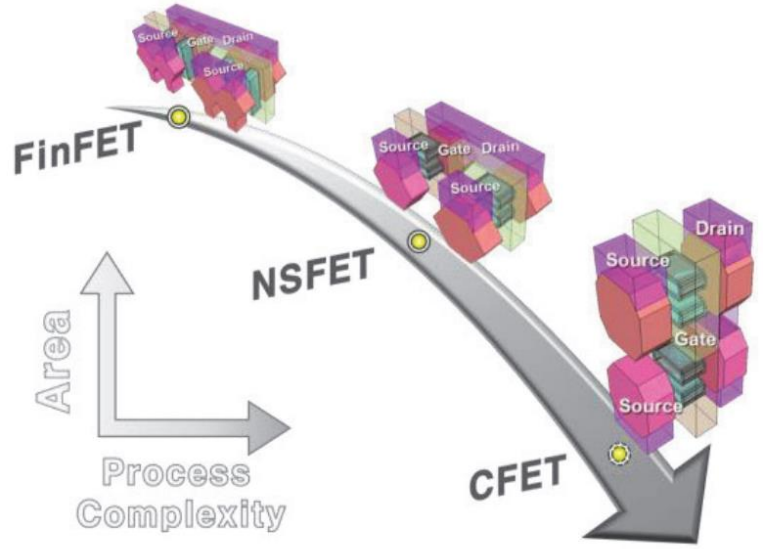

Figure 1. Semiconductor devices roadmap.
Liao, S., et al. "Complementary Field-Effect Transistor (CFET) Demonstration at 48nm Gate Pitch for Future Logic Technology Scaling." 2023 International Electron Devices Meeting (IEDM). IEEE, 2023.

Focus:

- State of the art review
  - Complementary Field Effect Transistor (CFET)
  - From FinFET to GAAFET to CFET: motivation
- Challenges and opportunities
  - Main manufacturing steps
  - Backside power delivery
  - Performance vs. design parameters
- Overview of published CFET devices

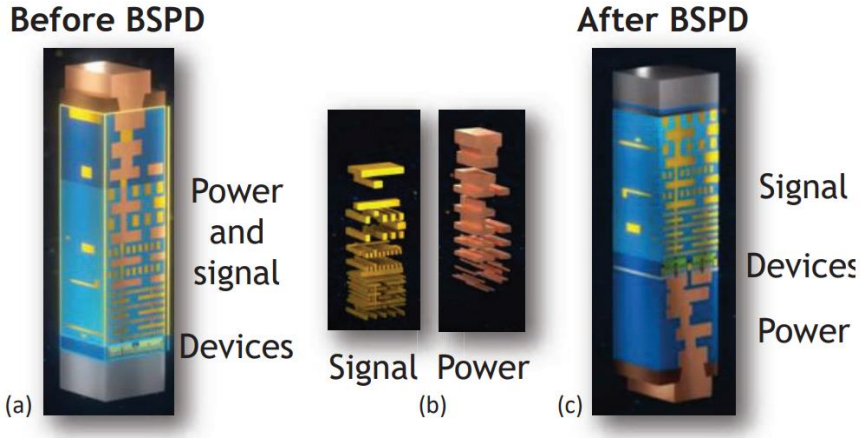

Figure 2. Impact of backside PDN.
Kobrinsky, M., et al. "Process Innovations for Future Technology Nodes with Back-Side Power Delivery and 3D Device Stacking." 2023 International Electron Devices Meeting (IEDM). IEEE, 2023.

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Dynamic Offset cancellation techniques:

Chopping vs Auto zeroing

Background:
At low frequencies, offset, 1/f noise and drift are the dominant error sources of operational amplifiers which need to be eliminated in high precision circuits.

Focus:

- Introduction to offset cancellation methods.
  - Static
  - Dynamic
- Analysis of dynamic offset cancellation techniques.
- Comparison of the pros and cons of each technique.
- Suggestions/example with modified circuitry for enhanced performance.

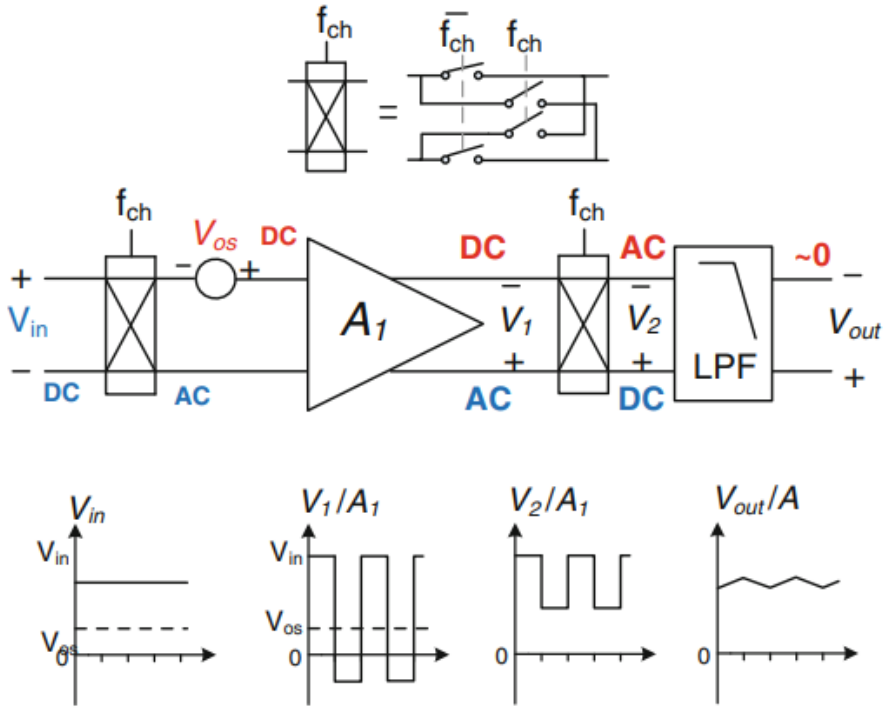

Fig. 1: An example of chopping based dynamic offset cancellation mechanism[1].

1 - R. Wu et al., Precision Instrumentation Amplifiers and Read-Out Integrated Circuits, Analog Circuits and Signal Processing, DOI: 10.1007/978-1-4614-3731-4_2, Springer Science+Business Media New York 2013

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Physical Unclonable Functions

State-of-the-Art, design and implementation, comparison

Background:

Physical Unclonable Functions (PUFs) represent a cutting-edge technology in the field of hardware security, providing unique fingerprints for electronic devices by leveraging manufacturing variations to produce unique responses. They are essential for cryptographic key generation, device authentication, and anti-counterfeiting.

Focus/Tasks:

- The most recent circuit implementations/different approach
- Comparison of implementations
- Classification
- Performance metrics
- Applications
- Challenges and future directions

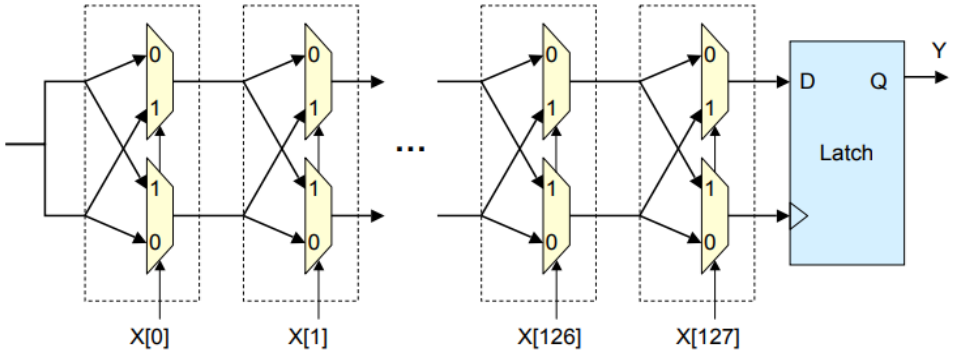

Figure 1: An arbiter PUF delay circuit. The circuit creates two delay paths with the same layout length for each input X, and produces an output Y based on which path is faster.

Source Figure 1: G. E. Suh and S. Devadas, "Physical Unclonable Functions for Device Authentication and Secret Key Generation," 2007 44th ACM/IEEE Design Automation Conference, San Diego, CA, USA, 2007, pp. 9-14.

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Physical Layer RF Fingerprinting for wireless devices

State-of-the-Art, implementation, comparison

Background:

Physical Layer Device Fingerprinting is a technique used to identify and distinguish devices based on their unique physical characteristics, such as hardware imperfections, at the physical layer of the OSI model. This technique has gained significant attention in recent years due to its potential applications in various fields, including device authentication, intrusion detection, and IoT security.

Focus/Tasks:

- Different approaches, comparison
- Performance metrics
- Applications
- Challenges and future directions

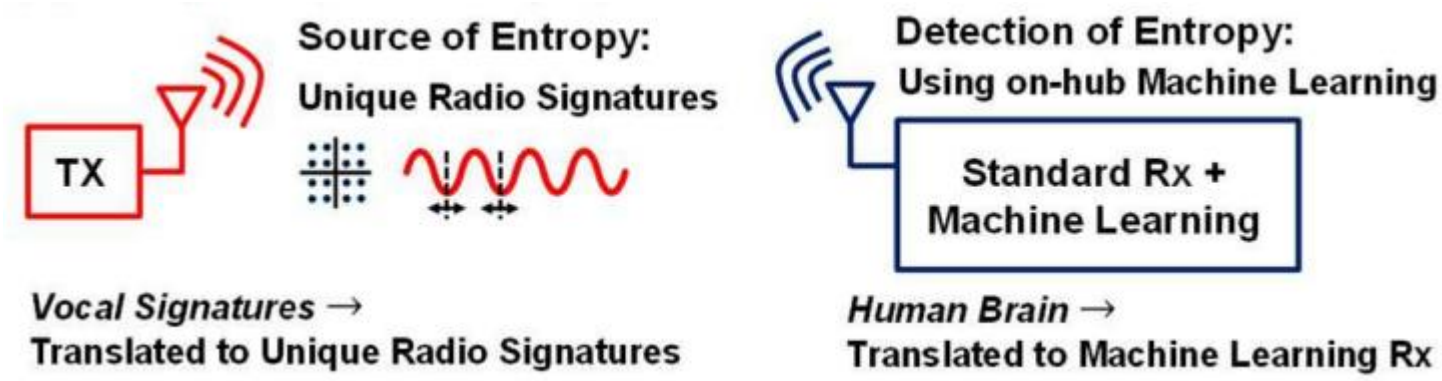

Figure 2: Proposed RF-PUF framework for secure radio communication

Source Figure 2: B. Chatterjee, D. Das, S. Maity and S. Sen, "RF-PUF: Enhancing IoT Security Through Authentication of Wireless Nodes Using In-Situ Machine Learning," in IEEE Internet of Things Journal, vol. 6, no. 1, pp. 388-398, Feb. 2019, doi: 10.1109/JIOT.2018.2849324.

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CD-Converter: Techniques, Efficiency, Flexibility

State-of-the-Art, Design, Features, Comparison

Problem:
Need for efficient capacitance to digit converter considering topology, effort and efficiency (area, noise, current, resolution)

Focus

- State-of-the-Art: CD-Converters
  - Topologies: Delta-Sigma, SAR, Dual-Slope
  - Conversion concept? Is it directly Cap to Digit?
  - Efficiency (FoM), Resolution, …
  - Limitations of topology
- Comparison of topologies
  - Advantages/Disadvantages
  - Highlighting of the crucial trade-offs
  - Comparison table

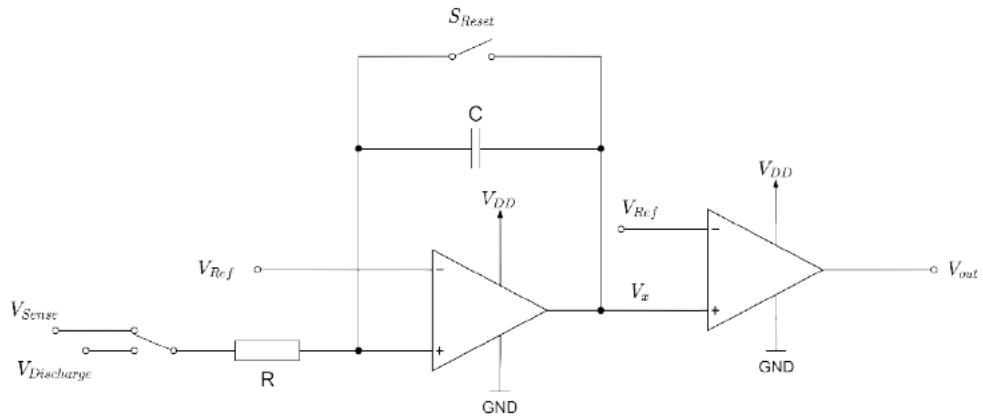

Figure 1. Dual-Slope Converter

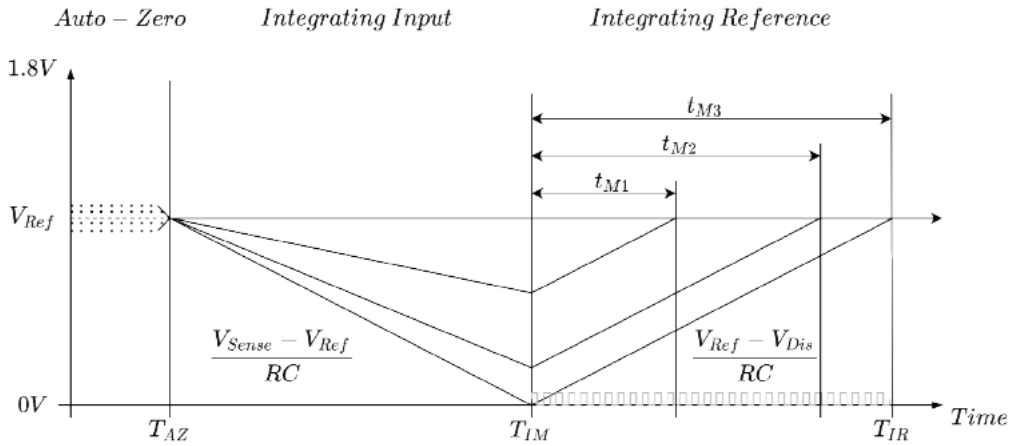

Figure 2. Typical dual-slope conversion cycle

Source Figure 1, 2: Analog-to-digital converter for the genration of keys with mechanical stress compensation, Tobias Chlan

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Electronic Tongues and Noses

Background:
Electronic tongues enable the correct differentiation of e.g. sweat samples from healthy and unhealthy patients via pattern recognition.

Focus:

- Literature Study of State-of-the-Art
- Focus on Environmental and Healthcare Applications
- Comparison of used Sensor arrays
  - Potentiometric Sensors
  - Impedimetric Sensors
  - Mixed Sensors
- Pattern recognition
- Current challenges

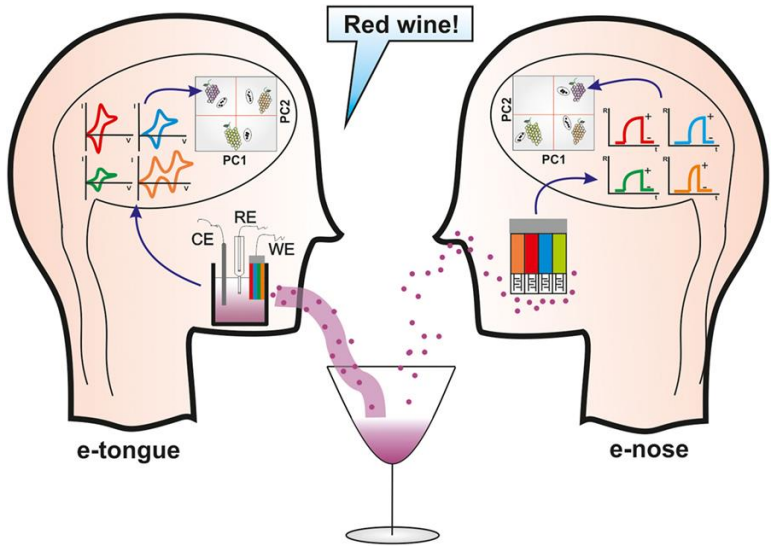

Figure 1. Example for an electronic tongue/nose system

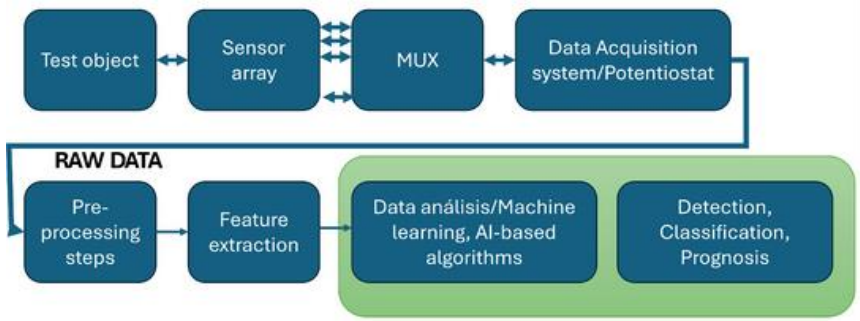

Figure 2. Data acquisition and analysis steps

Figure 1: https://www.frontiersin.org/articles/10.3389/fbioe.2016.00081/full
Figure 2: https://www.mdpi.com/2079-6374/14/4/190

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Cryogenic Circuit Design for Quantum Computing

Comparison between platforms, requirements and challenges

Background:
Most quantum computing systems are operated at cryogenic temperatures (<4 K). As a result, designers face challenges when designing qubit control circuits.

Focus:

- Overview of state-of-the-art literature for qubit control circuits
- Look at superconducting, spin qubit and trapped ion quantum computing
- Dominant approaches for each system
- What are particular challenges/requirements for each system, which challenges are similar or the same
  - How are these challenges addressed

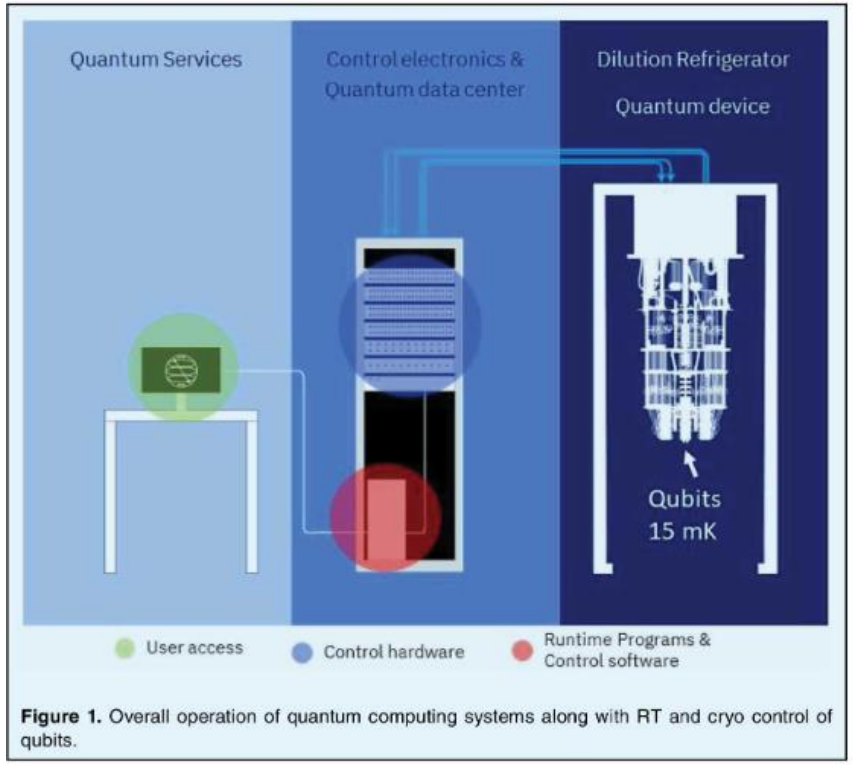

Figure 1. Overall operation of quantum computing systems along with RT and cryo control of qubits.

S. Chakraborty and R. V. Joshi, "Cryogenic CMOS Design for Qubit Control: Present Status, Challenges, and Future Directions [Feature]," in IEEE Circuits and Systems Magazine, vol. 24, no. 2, pp. 34-46

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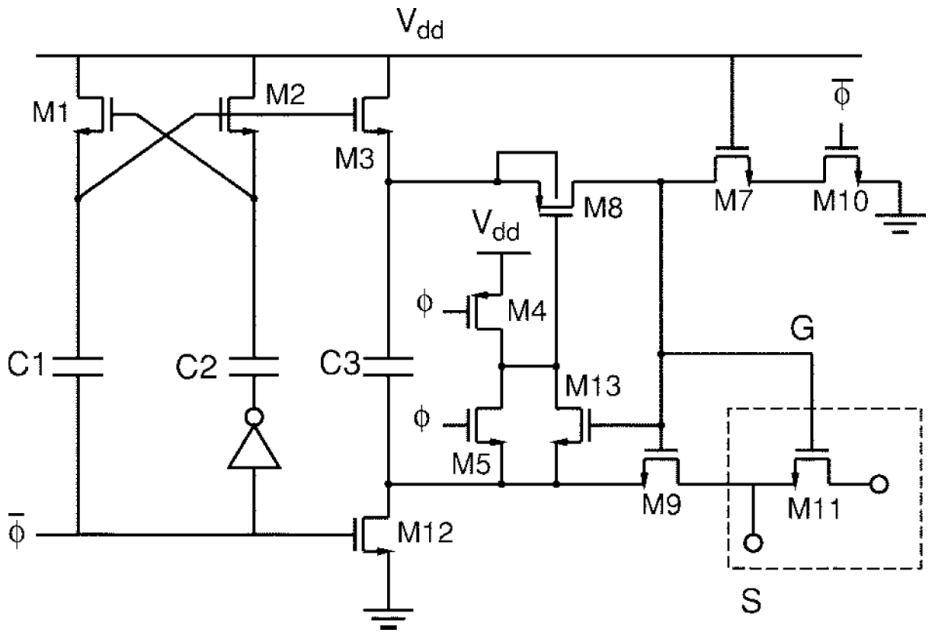
Low Distortion Switches for Sample-and-Hold Stages

Bootstrapped switches and compensation techniques

Background:
In trapped ion quantum computing many proposed architectures make use of heavy multiplexing of qubit control signals. This requires very accurate switches, similar to the application in sample and hold stages for data converters

Focus:

- Literature study of state-of-the-art
- Focus on switches designed for sample and hold stages in analog-to-digital converters
- Comparison of topologies
  - Accuracy/hold pedestal step
  - Area
  - Power consumption



Abo, A. M. and Gray, P. R., 1999. A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter. *IEEE Journal of Solid-State Circuits* , Vol. 34, No. 5.

Supervisor: ferdinand.pscheidl@tum.de

Neuromorphic Solutions for Control Problems

Background:
Biological neural networks solve complex and high-speed control problems with very low power consumption. Humming-birds are able to perform a stable position control by flapping their wings up to 60 times per second while moving with up to 100 km/h. Spiking Neural Networks (SNN) run on low latency neuromorphic hardware therefore have the potential to enable very energy efficient control of high-speed systems.

Focus/Tasks/Goals/Structure/etc.:

- How does the latency of a controller limit the speed of a control problem?
- Investigate state-of-the-art neuromorphic solutions for control problems
  - Which problems are tackled?
  - How are SNNs designed/trained to solve the problems?
  - What KPIs of neuromorphic hardware limits the applicability of SNNs for control problems?

https://www.birdsandblooms.com/birding/attracting-hummingbirds/how-fast-do-hummingbirds-fly/ , 23.09.2024

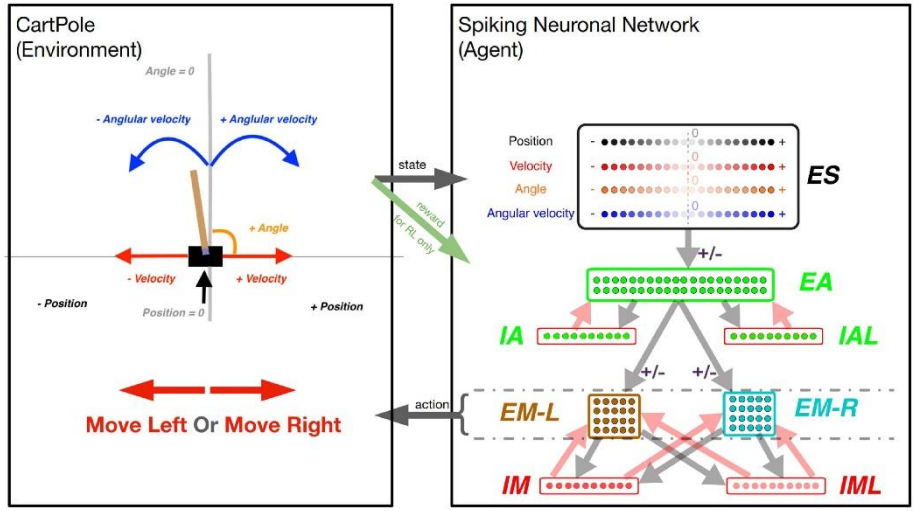


Figure 1. Haşegan D et. al. Training spiking neuronal networks to perform motor control using reinforcement and evolutionary learning. Front Comput Neurosci. 2022