Lehrstuhl für Schaltungsentwurf
Fakultät für Elektrotechnik und Informationstechnik
Technische Universität München

Scientific Seminar on Structure, Architecture, and Application of Sensor Circuits

Chair of Circuit Design

Summer Semester 2025

What you will learn in this seminar …

- At least 50% of this seminar is about the soft skills you need to become a successful engineer in science, but also in industry
- You will learn to:
  - Research state-of-the-art for a newly defined problem, and get a deeper understanding of the problem
  - Formulate a plan for solving the problem
  - Present technical work in a scientific paper, such that others can understand the content but also the motivation for the topic, what others have done in the field already, what you did new and better than others, as well as the remaining challenges after your work
  - Orally present the same topic to a group with the same intention

… **good work is often only recognized if it is also well presented (and for this, first of all,** it needs to be understood by others in a short time frame)!

Outline – Kick-Off Meeting

Today …

- Your work and duties during this seminar
- Timing & Deadlines: Submissions and presentations
- Grading of your work
- Presentation of topics by supervisors
- Selection of one topic per student
- Lecture: How to do literature research

Outline – Course of the seminar

- Then …
  - Lecture 2: How to write an article
  - Lecture 3: How to do a presentation
  - Work on your own: Text / Internet search / discussions
  - In case you need help: please contact your supervisor in advance and try to use your and his/her time efficiently
  - Take advantage of the supervisor's feedback, this is where you can learn most!
  - Show your results: report (4 pages) and oral presentation (12+3 min.)

Your work and duties

- Choose one of the topics
- Do research about the topic
- Write a scientific paper about the topic (4 pages)
- Prepare and give a scientific presentation (12 min + 3 min Q&A, this is the standard for conferences)
- For paper and presentation:
  - focus on basics of the problem and specific implementation
  - a template will be provided on Moodle

Your work and duties

1. Do a literature search and discuss your research results with your supervisor
2. Then study the literature
3. Develop an outline (content) for your paper and presentation
4. Discuss your outline with your supervisor (by appointment)
5. Work out the outline in your paper
6. Submit your paper
7. Summarize your results in a presentation
8. Submit the presentation

Grading

- ✓ Regular discussions (online/in presence) with the assigned supervisor about the progress of the work and the procedure
- ✓ Oral presentation of the results (12 min.) with subsequent discussion (3 min.) (50%)
- ✓ Scientific paper in IEEE style (4 pages): written elaboration of the results (50%)

Timing & Deadlines

	When?	What?
Kick-off	30.4.2025 15:00-17:00	Introduction & How to do a literature research **Participation is mandatory!**
Lecture 1	13.05.2025 15:30-17:00	How to write a scientific article
Lecture 2	25.06.2025 15:30-17:00	How to prepare and hold a presentation
Paper submission deadline	20.07.2025 (Monday) until 23:59 PM	In Moodle and via email to your supervisor
Presentations	23.07.2025, 10:30-12:30 23.07.2025, 14:00-16:00	

Topics (Overview)

Topic	Supervisor	Available
ESD Protection of D2D/D2W Interfaces	Emanuele Groppo	
Breaking the kT/C Noise Limit	Leon Dixius	
Neuromorphic Solutions for Control Problems	Ferdinand Pscheidl	
Voltage Regulator Design for Againsting Power Analysis Attacks	Pengcheng Xu	
Mechanical Stress Compensation in the Bandgap References Design	Pengcheng Xu	
N-Channel Programmable Analog Audio Filter for neuromorphic appproach	Marco Schewa	
Physical Unclonable Functions	Egla Derraj	
Power-on-Reset and Brown-out Detection Circuits	Moritz Gruber	
Concepts of Physical unclonable functions (PUFs)	Carl Riehm	
Circuits For Local Learning in Hardware-Implemented Spiking Neural Networks	Nikan Dehghan-Manschadi	

LAST UPDATED 31.03.2025

Supervisor: emanuele.groppo@tum.de

ESD Protection of D2D/D2W Interfaces

Problem:
Reduced area/capacitance budget for ESD protection of high-density die-to-die interfaces

Focus:

- State of the art review
  - Die-to-Die (D2D) and Die-to-Wafer (D2W)
  - Diode-based Electrostatic Discharge protection
- Challenges and opportunities
  - Origin and risk of Electrostatic Discharge
  - Area and capacitance constraints
  - Transient diode overshoot (forward recovery)
- Overview of devices and solutions

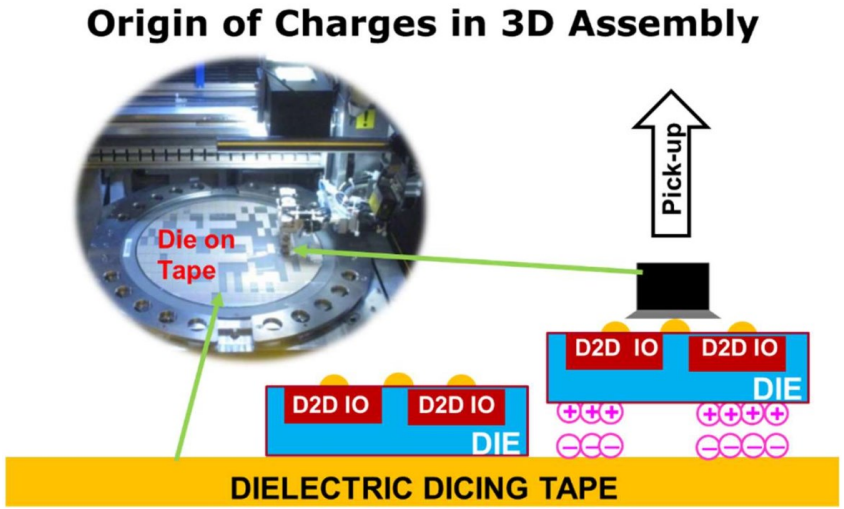


Figure 1. Electrostatic charging during D2D/D2W bonding procedure.
Industry Council On ESD Target Levels. "A Case for Lowering Component Level CDM ESD Specifications and Requirements Part II: Die-to-Die Interfaces." (2023).

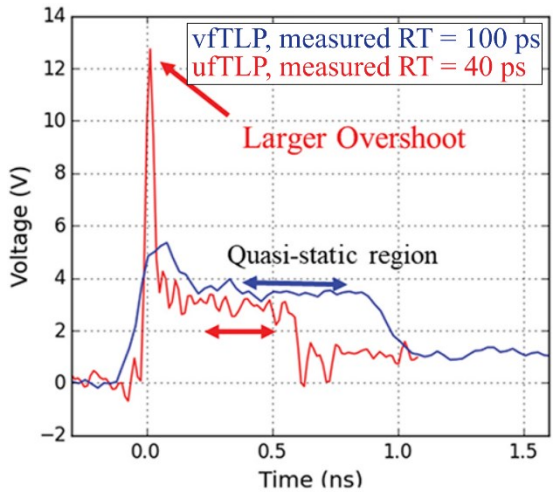


Figure 2. Impact of rise time on transient voltage overshoot in ESD protection diodes.
Ishfaq, Umair, et al. "Advanced CDM Simulation Methodology for High-Speed Interface Design." 2022 44th Annual EOS/ESD Symposium (EOS/ESD). IEEE, 2022.

Supervisor: leon.dixius@tum.de

Breaking the kT/C Noise Limit

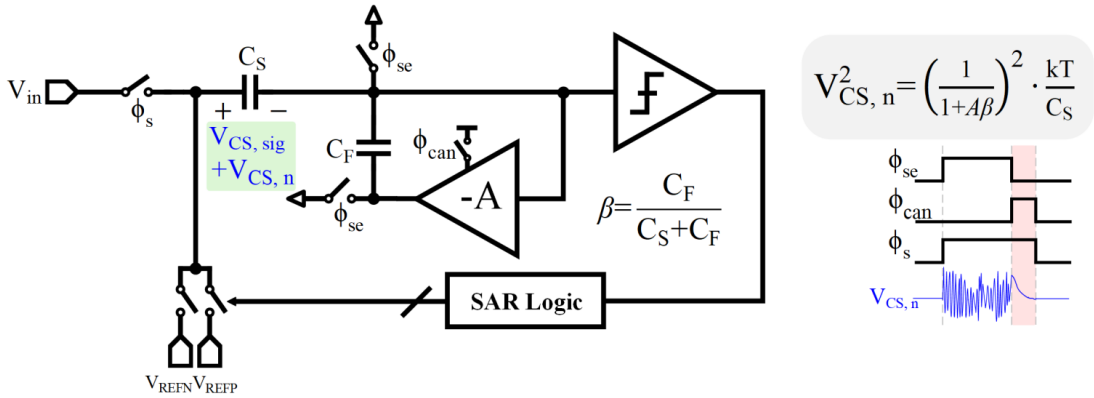
Sampling circuits with kT/C noise cancellation techniques

Background:

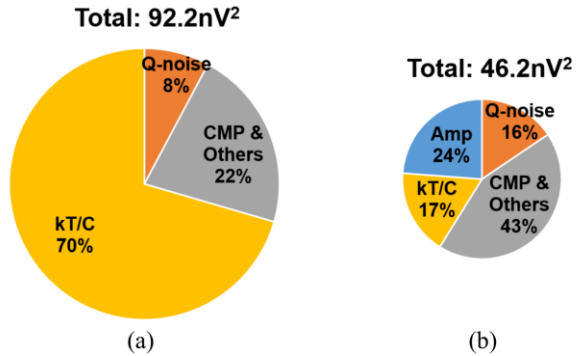
Thermal noise in switched capacitor (SC) circuits leads to the so called *kT/C* noise. This noise represents a major limitation in most SC circuits. To achieve a certain SNR, the sampling capacitor can be increased. However, this can lead to undesirable trade offs.

Focus:

- Literature study of state-of-the-art
  - Understanding *kT/C* noise
  - Trade offs, that this limitation implies
- Sampling circuits with *kT/C* noise cancellation
  - Overview and comparison



SAR ADC with kT/C noise cancellation using a feedback auxiliary amplifier



ADC noise breakdown (a) NC off and (b) NC on

Won, J., Son, B., et. al. 2024. A 13b 40MS/s SAR ADC with Robust kT/C Noise Cancellation using a Feedback Auxiliary Amplifier. *ESSERC*.

Supervisor: ferdinand.pscheidl@tum.de

Neuromorphic Solutions for Control Problems

Background:
Biological neural networks solve complex and high-speed control problems with very low power consumption. Humming-birds are able to perform a stable position control by flapping their wings up to 60 times per second while moving with up to 100 km/h. Spiking Neural Networks (SNN) run on low latency neuromorphic hardware therefore have the potential to enable very energy efficient control of high-speed systems.

Focus/Tasks/Goals/Structure/etc.:

- How does the latency of a controller limit the speed of a control problem?
- Investigate state-of-the-art neuromorphic solutions for control problems
  - Which problems are tackled?
  - How are SNNs designed/trained to solve the problems?
  - What KPIs of neuromorphic hardware limits the applicability of SNNs for control problems?

https://www.birdsandblooms.com/birding/attracting-hummingbirds/how-fast-do-hummingbirds-fly/ , 23.09.2024

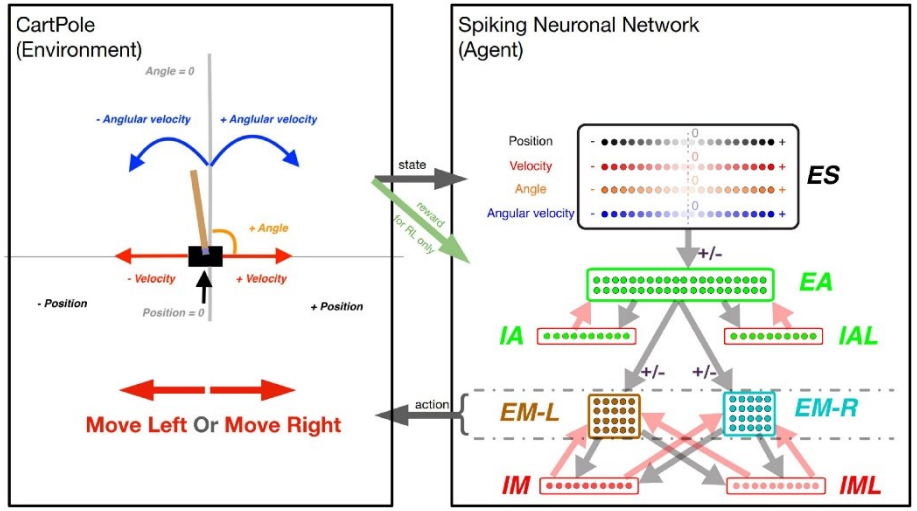


Figure 1. Haşegan D et. al. Training spiking neuronal networks to perform motor control using reinforcement and evolutionary learning. Front Comput Neurosci. 2022

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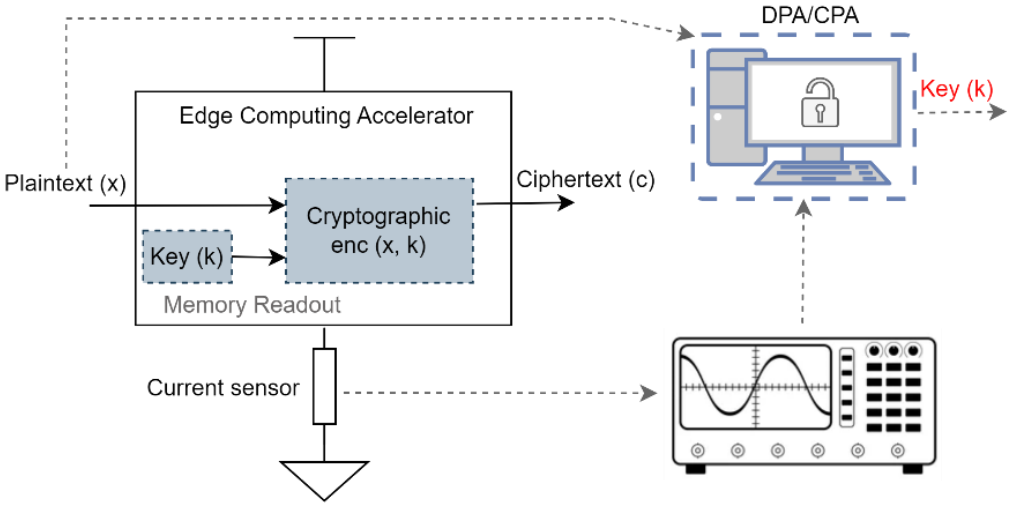
Voltage Regulator Design for Againsting Power Analysis Attacks

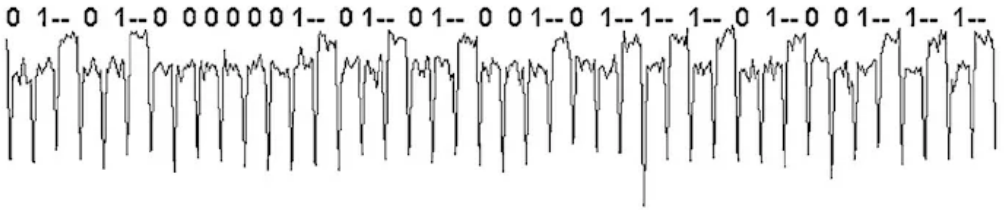
Design Principal Analysis and SOA Summary

In power-based side-channel attacks, an adversary observes the power current or voltage variations during the device's operation. In CMOS technology, the power consumption correlates with the activities being carried out by the device. Specifically, the energy usage of a circuit fluctuates depending on the actions of individual transistors. This relationship has revealed that the power consumption of an IC serves as a side channel, inadvertently exposing details about the internal operations, processed data, and activities occurring within the IC.



In this topic, you are expected to

- Summary and analysis the working principle of power analysis attacks (PAA) and the SOA work on voltage regulator design to against PAA.
- Summary and analysis the new feasure of PAA in edge devices.
- Summary the side channel analysis (SCA) attacks resistance measurement solutions and how SCA attacks resistance is measured from a voltage regulatro design.



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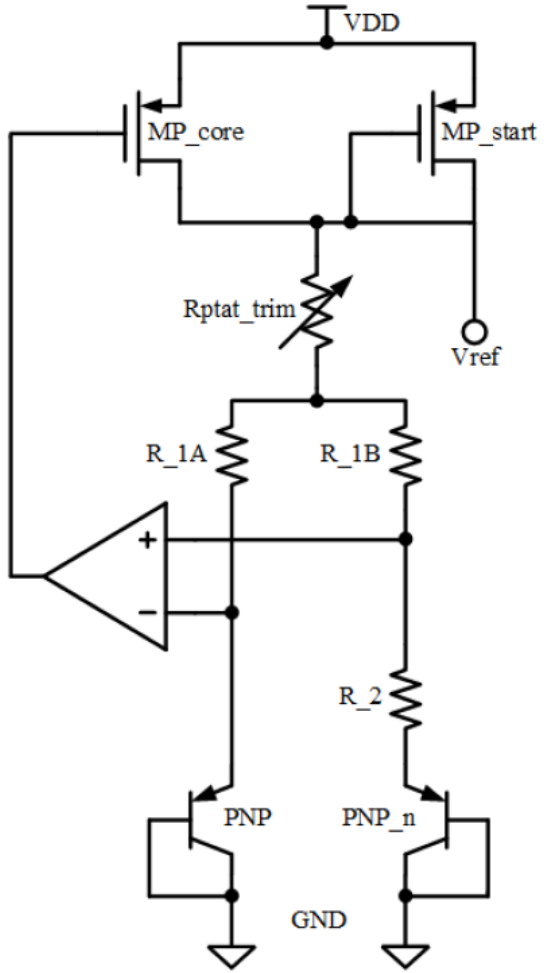
Mechanical Stress Compensation in the Bandgap References Design

Design Principal Analysis and SOA Summary

High accuracy of voltage references in analog integrated circuit is drawing increasing attention due to their reliability and scalability with modern advanced technology. According to the research, the dominant contributor to the rest inaccuracy is the mechanical stress effect introduced by packaging.

In this topic, you are expected to

- Summary the mechanical stress effect sources, model and its impact on CMOS bandgap circuit.
- Summary the working principle and SOA circuit design of the mechanical stress compensation.
- Analysis the advantage and limitation of the state-of-art works on low-power bandgap reference design.



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N-Channel Programmable Analog Audio Filter for neuromorphic appproach

Audio tasks, such as keyword spotting (KWS) or simple language understanding, have become an integral part of many voice-controlled devices. The neuromorphic approach needs a continuous-time (CT) N-Channel bandpass filter for processing.

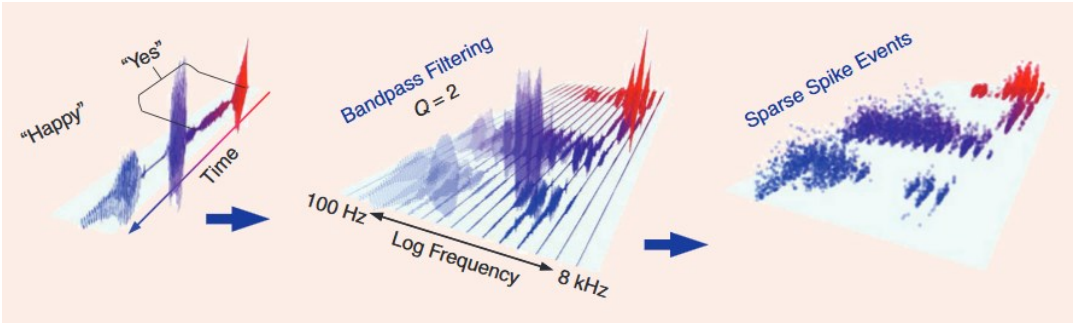

Figure 1. Audio Sample with audio processing after filtering

Task:

- Different N-Channel Audio Filter shall be compared
- Disadvantages and Advantages shall be shown as well as limits

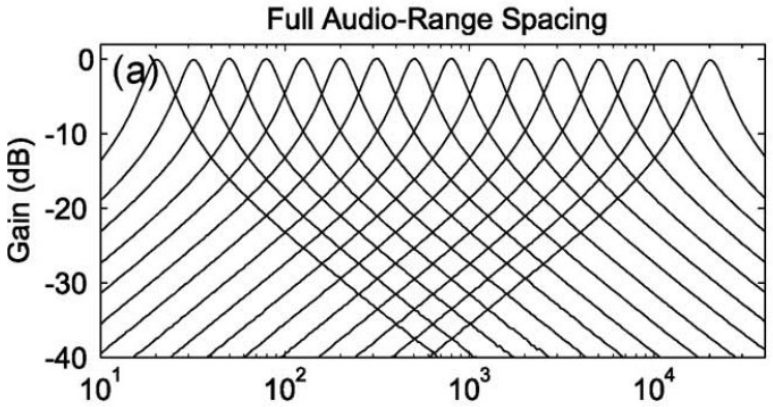

Figure 2. Cute n-Channel Bandpass Filter transfer function

Source Figure 1: Bringing Dynamic Sparsity to the Forefront for Low-Power Audio Edge Computing; C. Liu
Source Figure 2 A Low-Power and High-Precision Programmable Analog Filter Bank; B.Rumberg

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Physical Unclonable Functions

State-of-the-Art, design and implementation, comparison

Background:
Physical Unclonable Functions (PUFs) represent a cutting-edge technology in the field of hardware security, providing unique fingerprints for electronic devices by leveraging manufacturing variations to produce unique responses. They are essential for cryptographic key generation, device authentication, and anti-counterfeiting.

Focus/Tasks:
- The most recent circuit implementations/different approach
- Comparison of implementations
- Classification
- Performance metrics
- Applications
- Challenges and future directions

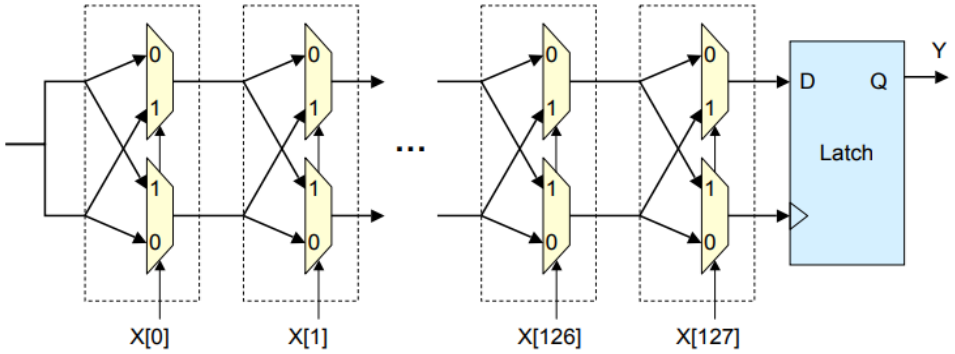

Figure 1: An arbiter PUF delay circuit. The circuit creates two delay paths with the same layout length for each input X, and produces an output Y based on which path is faster.

Source Figure 1: G. E. Suh and S. Devadas, "Physical Unclonable Functions for Device Authentication and Secret Key Generation," 2007 44th ACM/IEEE Design Automation Conference, San Diego, CA, USA, 2007, pp. 9-14.

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Power-on-Reset and Brown-out Detection Circuits

State-of-the-Art Techinques

Background:
Many systems need a defined behavior during start-up and shut-down. Power-on-Reset and Brown-out Detection circuits provide defined voltages/logic-levels during all supply voltages regimes, which can be used for initialization. Since these circuits constantly monitor the supply voltage and can therefore not be turned off, their power consumption is critical.

Tasks:

- Access the need of start-up circuits for initialization and shut-down of digital and analog circuits.
- Compare the State-of-the-Art of start-up circuits:
  - Find different topologies and techniques (e.g. resistor less, capacitive based).
  - Compare topologies and find tradeoffs (e.g. power consumption, area, …).

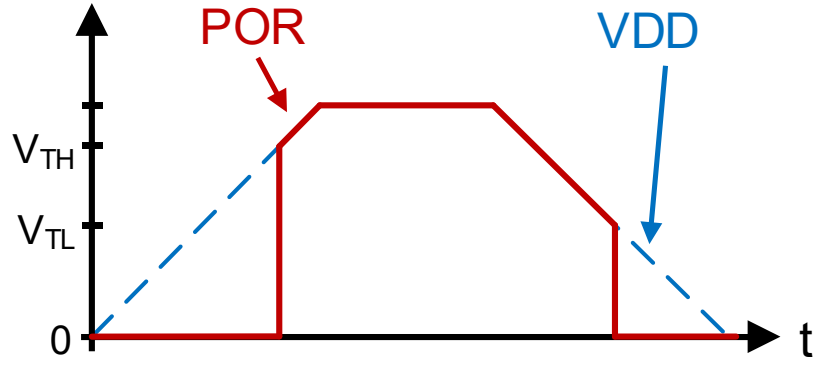

Figure 1. Startup behavior of a Power-on-Reset (POR) circuit. At VDD > V_{TH} the POR triggers. The Brown-out Detection triggers at V_{TL} (< V_{TH}).

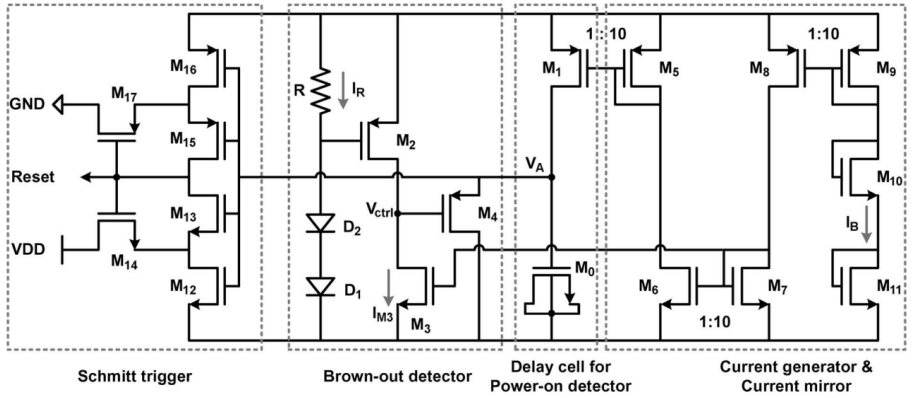

Figure 2. Example circuit of a Power-on-Reset (POR) circuit with Brown-out Detection.

Source Figure 2: Le, Huy-Binh, et al. "A long reset-time power-on reset circuit with brown-out detection capability." IEEE Transactions on Circuits and Systems II.

Concepts of Physical unclonable functions (PUFs)

Supervisor:
carl.riehm@tum.de

Problem: Mobile and embedded devices require to securely authenticate and be authenticated by another party. (e.g. financial transactions on a smartphone). Typically, secret authentication keys are stored in EEPROMs or SRAM cells. PUFs, however, exploit physical IC characteristics to generate a secret and reliable authentication key.

Figure 1. https://www.kaspersky.de/blog/fingerprints-sensors-security/6785/

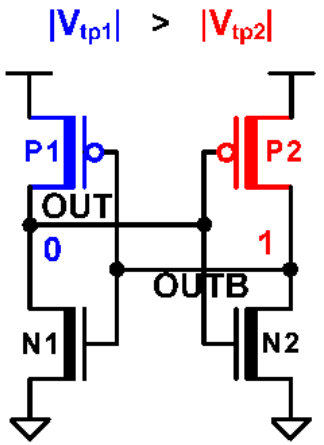

Figure 2. https://www.semanticscholar.org/paper/Design-of-SRAM-PUF-with-improved-uniformity-and-Garg-Kim/6851c6d0cec12f083d6002b06c337b1ac11cf02c/figure/1

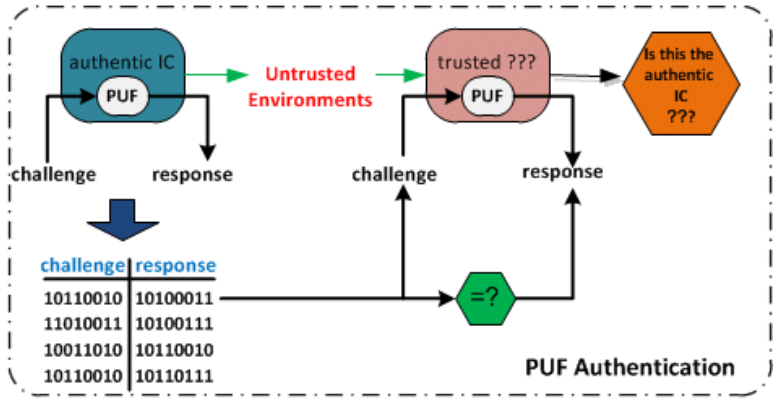

Figure 3. https://www.researchgate.net/figure/Physical-Unclonable-Functions-Secure-Authentication-Mechanism_fig1_319004864

Tasks/Focus:

- What approaches are used to create PUFs in standard CMOS processes?
- What are their advantadges/disadvantadges?
- Figure of merits to compare different concepts

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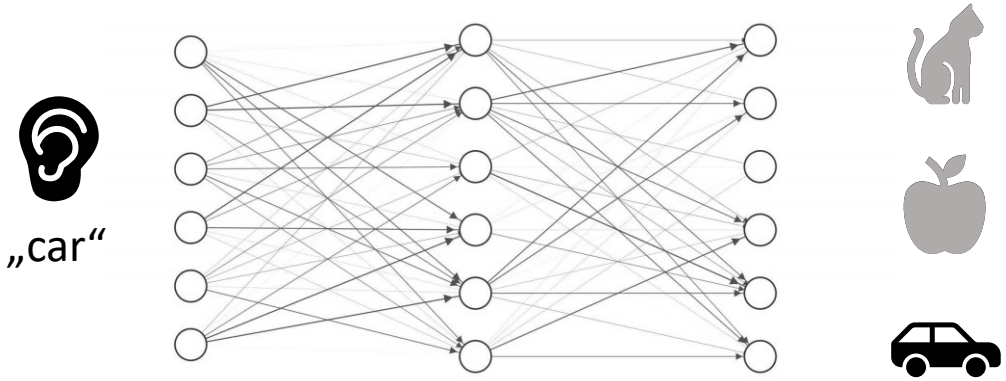
Circuits For Local Learning in Hardware-Implemented Spiking Neural Networks

Background:

- Spiking Neural Networks (SNN) are biological inspired Neural Networks that want to mimic the brain
- They use short electrical pulses, called „spikes“, to propagate information
- We can emulate and train them but „physical implementations“ with electronics are rare

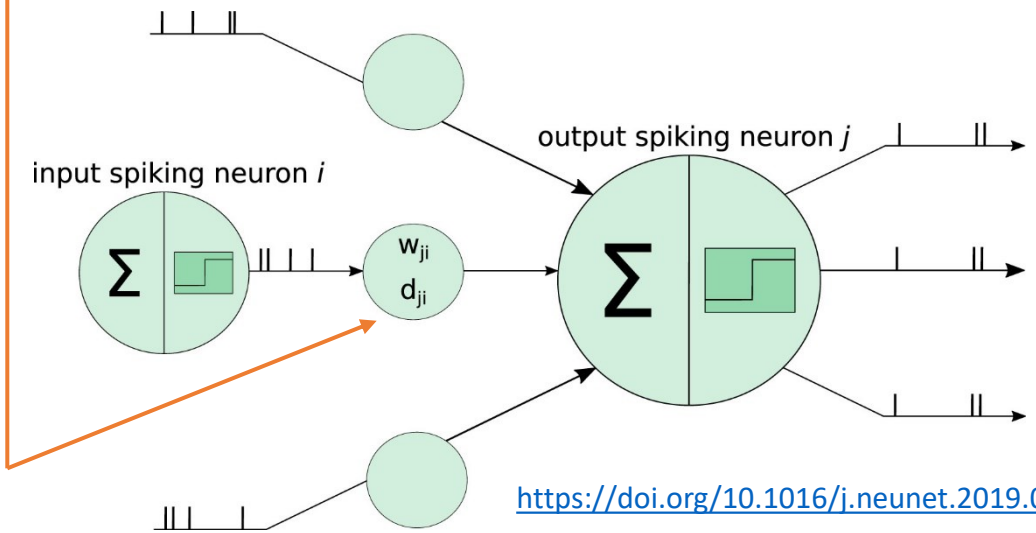
Goals:

- Understanding of SNNs and how SNNs learn in hardware
- Researching different learning rules and respective circuits that can do this in electronics
- Compare different approaches and highlight challenges



https://www.baeldung.com/cs/spiking-neural-networks

Learn by adapting weights in network



https://doi.org/10.1016/j.neunet.2019.09.004