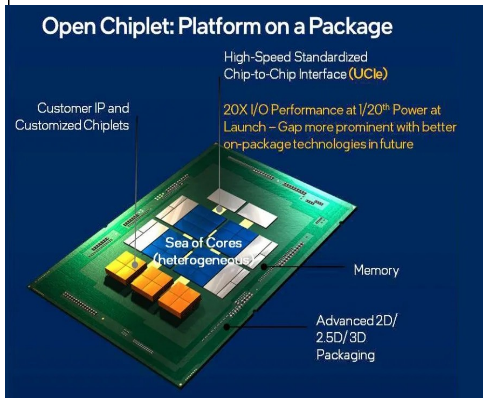
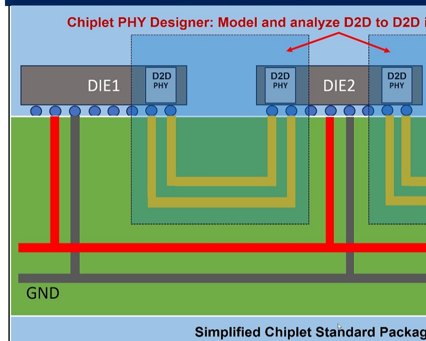
**Lehrstuhl für Schaltungsentwurf**
Fakultät für Elektrotechnik und Informationstechnik
Technische Universität München

# Inter-Chiplet-Communication

*Master-Thesis*

### *Motivation:*




A chiplet consists of multiple microchips inside one package. Contrary to a multi-die chip with bondwire connections, the chips in a chiplet are connected by interconnect traces that are part of the package. This enables more connections that use less space. Many communication standards like Improved Inter Integrated Circuit (I3C), Peripheral Component Interconnect Express (PCI), Serial Peripheral Interface (SPI) and Double Data Rate (DDR) take care of the communication between Chips on boards. The new standard Universal Chiplet Interconnect (UCIe) prioritizes interoperability among general-purpose chiplets.
In this master-thesis it should be investigated what can be used from the existing standards and what needs to be added or changed to achieve a flexible standard, that achieves low power for inter-chiplet sensor connections and high speed for inter-chiplet communication between digital chips.

### *What needs to be done?*

- Develope an understanding of existing communication protocolls
- Investigate Flexibility
- Focus on low power
- Investigate bus versus single ended structures
- Make a proposal for a communication standard

### *What are good prerequesties for this work?*

- Basic understanding of transmission line theory
- Basic knowledge of circuit design
- Interest in communication standards

| Become curious? → Contact: | Markus Dietl,<br>markus3.dietl@tum.de<br>Room N5309 |
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