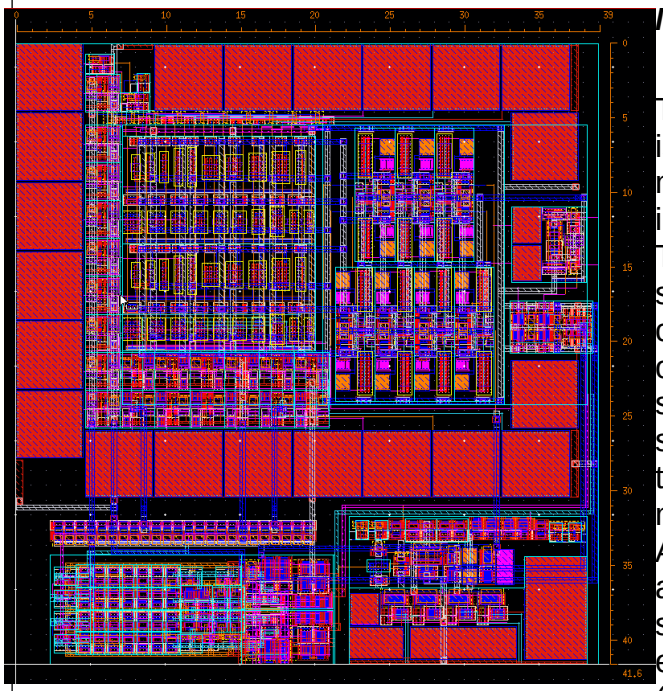
**Lehrstuhl für Schaltungsentwurf**
Fakultät für Elektrotechnik und Informationstechnik
Technische Universität München

# High Frequency PLL - Layout Influences

*Masterthesis*



***Motivation:***

The behaviour of high frequency PLLs is very often strongly influenced by the microchip layout. In this work this influence should be investigated.
The layout can be extracted and simulated. This simulation will consider most of the parasitic effects of the layout. The differences to a simulation only considering the schematic should be understood and the effect to the parameters of the modelling should be described .
An existing circuit should be layouted and depending on the outcome of the simulation, be modified using a design environment for integrated circuits (Cadence).

***What needs to be done?***

- Develope an understanding of the Phase Locked Loop
- Modelling of PLL
- Layout & Simulation of extracted layout
- Investigate the influence to the parameters in the Modelling of PLL
- Change the design to compensate for parasitic layout effects

***What are good prerequesties for this work?***

- Basic understanding of fourier transformation
- Basic knowledge of circuit design
- Intrest in circuit design & layout & modelling

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| Become curious? | → Contact: | Markus Dietl,<br>markus3.dietl@tum.de<br>Room N5309 |